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| **Course Name:** | **Linear Integrated Circuits and Design** | **Semester:** | **V** |
| **Date of Performance:** | **/08/2020** | **Batch No:** | **B1** |
| **Faculty Name:** | **Prof. MILID MARATHE** | **Roll No:** | **1912052** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **/25** |

**Experiment No: 6**

**Title:Implementation of Sample and Hold Circuit using High Speed Opamp**

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| **Aim and Objective of the Experiment:** |
| To implement and analyze sample and hold circuit using Opamp IC LTC6244   * To study and understand operation of sample and hold circuit and sampling of a given signal. * To analyze some performance parameters of sample and hold circuit. |

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| **COs to be achieved:** |
| **CO2:** Design circuits using opamp as linear applications. |

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| **Theory:** |
| A Sample and Hold Circuit, sometimes represented as S/H circuit is usually used with an Analog to Digital Converter to sample the input analog signal and hold the sampled signal. They are a critical part of Analog to Digital Converters and help in accurate conversion of analog signals to digital signals.In the S/H Circuit, the analog signal is sampled for a short interval of time. After this, the sampled value is hold until the arrival of next input signal to be sampled.  **Need of Sample and hold circuit:**  If the input analog voltage of an ADC changes more thanLSB, then there is a severe chance that the output digital value is an error. For the ADC to produce accurate results, the input analog voltage should be held constant for the duration of the conversion. As the name suggests, a S/H Circuit samples the input analog signal based on a sampling command and holds the output value at its output until the next sampling command is arrived.  **Performance Parameters:**  The performance of an S/H Circuit can be characterized by parameters that are commonly used for an amplifier like Input Offset Voltage, Gain Error, Non-linearity and so on. But there are a few characteristics that are specific to the S/H Circuits like Acquisition Time, Aperture Time, Hold Mode Settling Time, Hold Step, & Voltage droop.  These characteristics are helpful in analyzing its performance during the transition from sampling mode to hold mode (and vice versa) and also during hold mode operations. |

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| **Circuit Diagram:** |
| **Sample and hold Circuit:** |

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| **Stepwise-Procedure:** |
| 1. Make the sample & hold circuit schematic in LTspice.  2. Give sine wave input of amplitude , frequency of , and with a DC shift of .  3. Select LTC6244 as high speed opamp, from component library in LTspice.  4. Select switching device as MOSFET with periodic square control pulses of period .  5. Hold capacitor value is , and sampling time for the circuit is 0.1msec. (i.e 10 samples per cycle)  6. Simulate the circuit in transient domain, and plot input, control pulses & output waveforms of the circuit.  7. Repeat step 6, with 20 samples per cycle i.e control pulse period is .  8. Observe the changes in the output waveforms of the circuit with increased number of the samples per cycle. |

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| **Waveforms:** |
| **1:Input- Output and Control signal Waveform for (S/H) Circuit with 10 Samples/cycle:** |
| **2: Input- Output and Control signal Waveform for (S/H) Circuit with 20 Samples/cycle:** |
| **3: Expanded view of Input- Output and Control signal Waveform for (S/H) Circuit showing Acquisition time** |
| **4. Expanded view of Input- Output and Control signal Waveform for (S/H) Circuit showing Voltage Drooping** |

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| **Post Lab Questions:** |
| 1. What is the need of high speed opamp in a Sample and hold circuit?   **Ans:-**  low bias current FET input op amps are useful in sample-and- hold (SHA) circuits and peak detectors. Current feedback op amps have low voltage noise, high bandwidths, and fast settling times while maintaining unity- gain stability.   1. Explain Acquisition Time, Hold Step, & Voltage droop.   Ans:- Acquisition time (sampling time) is the time required for the Analog-to-Digital Converter (ADC) to capture the input voltage during sampling.  Voltage droop is the intentional loss in output voltage from a device as it drives a load   1. Change the value of to a higher value (say ), plot the pulse, input & output waveforms.      1. What is the effect of increased value of hold Capacitor on acquisition time and voltage droop.   Ans:- Droop can be reduced by increasing the value of the hold capacitor, but this will also increase acquisition time and reduce bandwidth in the track mode |

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| **Conclusion:** |
| **and analyze sample and hold circuit using Opamp IC LTC6244** |

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| **Signature of faculty in-charge with Date:** |